Research of Readout System for CEPC Semi-Digital Hadronic Calorimeter

# **Introduction**

After the discovery of the Higgs boson, it is natural to measure its properties as precise as possible. To obtain large number of Higgs boson, collider experiments are essential such as the running Large Hadron Collider (LHC). Besides LHC, scientists are propose to build future high energy collider such as International Linear Collider (LHC), Compact Linear Collider (CLIC), Future Circular Collider (FCC) and Circular Electron Positron Collider (CEPC). Calorimeters play an important role in modern collider system and for hadronic measurement sampling calorimeter is the best choice due to its fine segment and high spatial resolution. For hadronic calorimeter, usually use steel as absorber layer and gas detector or scintillator as active layer.

Simulation results show that for a calorimeter with cell sizes as small as 1×1 cm2, simple hit counting is already a good energy measurement for hadrons in the energy range of final state particles for the CEPC[[1]](#endnote-1). The probability for more than one charged particle hitting the same readout pad in-creases for higher energy, especially in the central region of a shower. A more general calorimeter with multi-threshold readout (e.g.3 thresholds) is therefore also considered, a so-called Semi-Digital Hadron Calorimeter (SDHCAL).

For CEPC HCAL, Gaseous Electron Multipliers (GEM) detector have been proposed for the active layers due to its high efficiency, high rate capability, homogeneity and compactness. The readout pads is sized 1×1 cm2, and for entire HCAL the readout channel density might be. So that the data acquisition system must be carefully designed.

# **Readout ASIC**



Figure 1 Structure of MICROROC ASIC

An ASIC named MICROROC (MICRO-mesh gaseous structure Read-Out Chip) is chosen to readout such huge channels. MICROROC is a 64 channels readout integrated circuit developed at IN2P3 by OMEGA/LAL and LAPP microelectronics groups[[2]](#endnote-2). The structure block of MICROROC is shown in figure 1. Each channel of MICROROC is made of a very low noise charge preamplifier, two different adjustable shapers (A high gain shaper for small signal and a low gain shaper for large signal), three comparators for tri-threshold readout and a random access memory used as a digital buffer. Other blocks, like 10-bit DAC, configuration register, bandgap voltage reference, LVDS receiver are shared by 64 channels.

# **Data Acquisition System**

The readout system structure is developed on SRS[[3]](#endnote-3) (the Scalable Readout System) proposed by the RD51 Collaboration. Similar with SRS, the readout system contains 3 main parts, a front-end board (FEB), a detector Interface board (DIF) and data acquisition card (DAQ). The structure of the whole system is shown in Figure 2.



Figure 2 Structure of readout system

The FEB (also called ASU-Active Sensor Unit) carries all the front-end ASIC, and in the future design it will be together with the readout plane of GEM detector. The DIF board is in charge of ASIC control and data connection, which is plugged to FEB using high density connector. The DAQ card is design to serve serval DIF boards. It distributes the clock, command and trigger to different DIF and gather the data from board.

Figure 3 Block of Phase I design

As shown in figure 3, a phase-I design is completed to verify this kind of readout structure and to test the performance of the MICROROC chip. A double layers GEM detector using self-stretching technology is used. The effective area is and the size of readout pad is 1. Figure 4(a) shows the readout plane of GEM detector. In this stage the readout ASIC is separated from the readout plane and a front-end board is designed to mount the ASIC. The front-end ASIC board is composed by 4 ASIC controlled by daisy chain. The DIF board controls the front-end ASIC board and transmit data to the upper board. The main controller of DIF is Xilinx A7 100T series FPGA. The data can be readout via USB2.0 or fiber-optical or Gigabit Ethernet or LVDS connector. Figure 4(b) shows the picture of FEB and the DIF board. All these PCBs are connected via kapton connector.

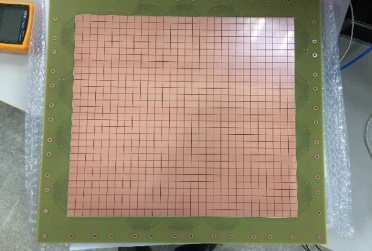


Figure 4 (a) Picture of readout plane

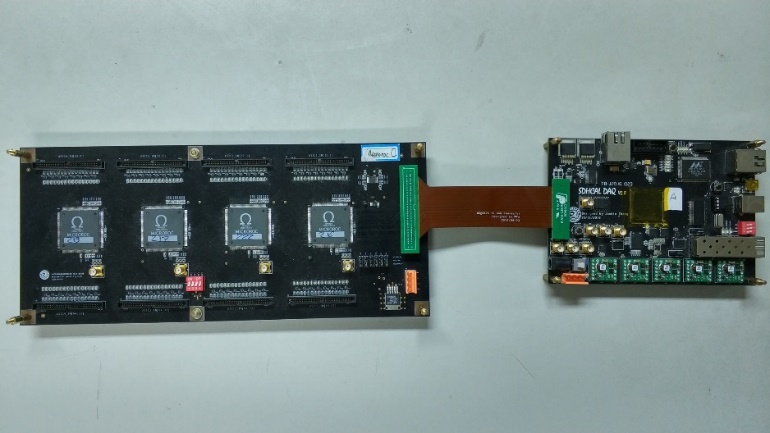


Figure 4 (b) Picture of FEB and DIF board

# **Calibration and Test**

The calibration method enables the digital readout system test automatically.

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# **Conclusion**

# **Reference:**

1. Ahmad, M. (2015). CEPC-SPPC preliminary conceptual design report, volume I: physics and detector. [↑](#endnote-ref-1)
2. Adloff, C., Blaha, J., Chefdeville, M., Dalmaz, A., Drancourt, C., Dulucq, F., ... & Karyotakis, Y. (2012). MICROROC: MICRO-mesh gaseous structure Read-Out Chip. Journal of Instrumentation, 7(01), C01029. [↑](#endnote-ref-2)
3. Martoiu, S., Muller, H., Tarazona, A., & Toledo, J. (2013). Development of the scalable readout system for micro-pattern gas detectors and other applications. Journal of Instrumentation, 8(03), C03015. [↑](#endnote-ref-3)